THAT WHICH IS CLAIMED IS:

1. Integrated structure (100; 100') in a chip of semiconductor material comprising:

a substrate (101) with a first type of conductivity;

an epitaxial layer (102) grown on said substrate and having a conductivity of the first type, the epitaxial layer having a conductivity less than the conductivity of the substrate;

a first region (104) and a second region (105) included in the epitaxial layer and having a conductivity which is opposite to that of the layer; said first and said second regions extending from a surface of the epitaxial layer opposite the substrate into the layer so as to form a first and a second junction with said layer;

means for reducing an injection of current through the layer from said first to said second region when the first junction is directly biased;

characterized in that said means comprise an isolating element (107) arranged between said first and said second region and extending from said surface of the epitaxial layer substantially at least as far as the substrate.

2. Integrated structure according to Claim 1, wherein said isolating element comprises a trench extending from said surface of the epitaxial layer as far as the substrate and filled with dielectric material.

3. Integrated structure according to Claim 1, wherein said isolating element is such as to surround partly said first region.

4. Integrated structure according to Claim 1, wherein said isolating element is such as to surround said second region.

5. Integrated structure according to Claim 1, wherein said isolating element has a length substantially equal to the width of said chip and divides the chip into two portions each including said first and said second regions.

6. Integrated structure according to Claim 2, wherein said trench includes polycrystalline silicon (203) for ensuring the planarity of the integrated structure.

7. Integrated structure according to Claim 1, wherein said substrate and said layer have a conductivity of the P type.

8. Integrated structure according to any one of Claims 1 to 7, wherein said first region comprises a power transistor (209, 208, 105) intended to control an inductive load having the collector region in said first region.

9. Method for the production of integrated structure comprising the steps of:

providing a substrate having a first type of conductivity;

growing on said substrate an epitaxial layer having a conductivity of the first type, said conductivity of the epitaxial layer being less than the conductivity of the substrate;

forming, inside the substrate, a first and a second region having a conductivity opposite to that of the epitaxial layer; said first and second regions extending from a surface of said epitaxial layer opposite the substrate into the said epitaxial layer so as to form, together with the epitaxial layer, a first and a second junction;

providing means for reducing an injection of current through the layer from said first to said second region when said first junction is directly biased;

characterized in that said step of providing means for reducing the injection of current comprises a step involving arrangement, between said first and second regions, of an isolating element extending from said surface of the epitaxial layer substantially at least as far as the substrate.

10. Method according to Claim 9, wherein said step of arranging an isolating element in between comprises a step involving formation of a trench extending from said surface of the epitaxial layer substantially at least as far as the substrate.

11. Method according to Claim 10, moreover comprising a step involving filling said trench with dielectric material.